ABSTRACT

An integrated memory has individually addressable normal and redundant units of memory cells. A memory unit is used to store, in a normal mode, an address for one of the normal units which needs to be replaced by one of the redundant units. A comparison unit compares an address which is present on an address bus with an address stored in the memory unit and activates one of the redundant units in the event of a match being identified. The memory also has a test circuit which can be activated by a test mode signal, can reset the memory unit to an initial state, and can store an address for one of the redundant units in the memory unit for subsequently writing an identification code to this redundant unit.